## REMARKS

*Cancelled Claims*

Claim 13 is herein cancelled without prejudice or disclaimer. The Applicant reserves the right to re-introduce claim 13 in continuation applications of the present Application.

*Rejections Under 35 U .S. C. § 102*

Claims 9-14, 15-19, 20, 23-25, 33-38, and 42-48 were rejected under 35 U.S.C. § 102(e) as being anticipated by Matsuo et al. (U. S. Patent No. 5,923,827).

Applicant respectfully traverses this rejection. Applicant reserves the right to swear behind the reference Matsuo et al., but feels that claims 9-12, 14, 15-19, 20, 23-25, 33-38, and 42-48, as amended, are allowable for the following reasons.

Applicant respectfully maintains that Matsuo et al. teaches a Flash memory having erase blocks management system for a facsimile machine where each erase block has a management area in a first memory block that is dedicated to management of the other 63 memory blocks of the erase block and does not contain user data. Applicant maintains therefore that Matsuo et al. does not teach or disclose a Flash memory that has an erase block management data structure in the control data sections of a subset of sectors of each erase block. *See, e.g.,* Matsuo et al., Figure 2, and column 5, line 58 to column 6, line 5.

As such, Applicant submits that Matsuo et al. fails to teach a Flash memory that has an erase block management data structure in the control data sections of a subset of sectors of each erase block.

Applicant's claim 9 is directed to a Flash memory device comprising a memory array containing a plurality of floating gate memory cells divided into a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, and an erase block management data structure arranged in the control data sections of a first set of sectors of each erase block of the plurality of erase blocks. As

detailed above, Applicant submits that Matsuo et al. fails to teach at least these limitations.

Applicant's claim 15 is directed to a Flash memory device comprising a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, and an erase block management data structure arranged in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks, wherein each erase block of the plurality of erase blocks has an erase block state that is recorded in the erase block management data structure of the erase block. As detailed above, Applicant submits that Matsuo et al. fails to teach at least these limitations.

Applicant's claim 20 is directed to a Flash memory device comprising a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section; a control circuit; and an erase block management data structure arranged in the control data sections of a first set of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that Matsuo et al. fails to teach at least these limitations.

Applicant's claim 33 is directed to a method of operating a Flash memory device comprising storing an erase block management data structure in each erase block of a plurality of erase blocks of a Flash memory array, wherein each erase block contains a plurality of sectors and the erase block management data structure of each erase block is stored in a plurality of control data sections of a subset of the plurality of sectors. As detailed above, Applicant submits that Matsuo et al. fails to teach at least these limitations.

Applicant's claim 42 is directed to a method of operating a Flash memory device comprising placing an erase block management data structure in a control data section of a subset of sectors of a plurality of sectors of each erase block of a plurality of erase blocks of a Flash memory array, and recording an erase block state in the erase block management data structure in the control data section of the subset of sectors of each

erase block of the plurality of erase blocks. As detailed above, Applicant submits that Matsuo et al. fails to teach at least these limitations.

Applicant respectfully contends that claims 9-12, 14, 15-19, 20, 23-25, 33-38, and 42-48, as amended, have been shown to be patentably distinct from the cited reference. As claims 10-12, 14, 16-19, 23-25, 34-38, and 43-48 depend from and further define claims 9, 15, 20, 33, and 42 respectively they are also considered to be in condition for allowance. Claim 13 has been cancelled above without prejudice or disclaimer. Accordingly, Applicant respectfully requests allowance of claims 9-12, 14, 15-19, 20, 23-25, 33-38, and 42-48.

Claims 4-6, 8, 26-29, 32, 39, and 41 were rejected under 35 U.S.C. § 102(e) as being anticipated by Sassa et al. (U.S. Patent No. 6,144,607).

Applicant respectfully traverses this rejection. Applicant reserves the right to swear behind the reference Sassa et al., but feels that claims 4-6, 8, 26-29, 32, 39, and 41, as amended, are allowable for the following reasons.

Applicant respectfully maintains that Sassa et al. teaches a memory management system for high speed usage that does not need a time consuming initialization process. In Sassa et al., erase block management information is stored in a redundant area of every memory page of an erase block. In addition, each memory page contains a copy of the same management information in its redundant area, except for the last memory page which contains other additional management information for the erase block. Applicant maintains therefore that Sassa et al. does not teach or disclose a Flash memory that has an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. *See, e.g.,* Sassa et al., Figures 3A-3C, column 4, line 59 to column 5, line 10.

As such, Applicant submits that Sassa et al. fails to teach a Flash memory that has an erase block management data structure in the control data sections of a subset of sectors of each erase block.

Applicant's claim 4 is directed to a Flash memory device comprising a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further arranged into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section; and an erase block management data structure arranged in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that Sassa et al. fails to teach at least these limitations.

Applicant's claim 26 is directed to a system comprising a host coupled to a Flash memory device, wherein the Flash memory device comprises a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, and an erase block management data structure arranged in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that Sassa et al. fails to teach at least these limitations.

Applicant's claim 32 is directed to a method of making a Flash memory device comprising forming a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section; and forming an erase block management data structure in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that Sassa et al. fails to teach at least these limitations.

Applicant's claim 39 is directed to a method of operating a Flash memory device comprising storing a fault tolerant erase block management data structure in a plurality of sectors of each erase block of a plurality of erase blocks of a Flash memory array, wherein each erase block contains a plurality of sectors and the erase block management data structure of each erase block is stored in a plurality of control data sections of a subset of the plurality of sectors. As detailed above, Applicant submits that Sassa et al. fails to teach at least these limitations.

Applicant respectfully contends that claims 4-6, 8, 26-29, 32, 39, and 41, as amended, have been shown to be patentably distinct from the cited reference. As claims 5-6, 8, 27-29, and 41 depend from and further define claims 4, 26, 32, and 39 respectively they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests allowance of claims 4-6, 8, 26-29, 32, 39, and 41.

*Rejections Under 35 U.S.C. § 103*

Claims 7 and 40 were rejected under 35 U. S. C. § 103(a) as being unpatentable over Sassa et al., in view of Duke (U. S. Patent 3,576,982). Applicant respectfully traverses this rejection and feels that claims 7 and 40 are allowable for the following reasons.

Applicant respectfully disagrees with the Examiner and notes that, as stated above in regards to the rejection of independent claims 4 and 39 which claims 7 and 40 depend from, Sassa et al. fails to teach a Flash memory that has an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. As such, Sassa et al. fails to teach or disclose independent claims 4 and 39 and therefore does not teach or disclose all elements of claims 7 and 40. In addition, Duke also does not teach an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. Therefore combining the elements of Sassa et al. with Duke does not teach or disclose all elements of claims 4 and 39. The Applicant therefore maintains that claims 4 and 39 are thus allowable over Sassa et al. and Duke, either alone or in combination. As claims 7 and 40 depend from and further define claims 4 and 39, claims 7 and 40 are also deemed allowable.

Furthermore, in order to support a rejection under 35 U.S.C. § 103(a), Sassa et al.'s principle of operation would have to be modified. The Applicant maintains that Sassa et al. teaches storage of identical copies of management information in each redundant area of each memory block of an erase block in the interest of speed, reduction of initialization time, and redundancy. Applying the 1's complement data storage of Duke to the management information storage of Sassa et al. would change Sassa et al.'s principal of operation for storing management information. Therefore, Sassa et al. cannot

be used to support a rejection under 35 U.S.C. § 103 because MPEP § 2143.01 provides that if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious.

Applicant respectfully contends that claims 7 and 40 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 7 and 40.

Claims 21, 22 and 49 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuo et al., in view of Applicant's Admitted Prior Art (AAPA). Applicant respectfully traverses this rejection and feels that claims 21, 22 and 49 are allowable for the following reasons.

Applicant respectfully disagrees with the Examiner and notes that, as stated above in regards to the rejection of independent claims 20 and 42 which claims 21, 22 and 49 depend from, Matsuo et al. fails to teach a Flash memory that has an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. Matsuo et al. stores management information in a dedicated first memory block that does not contain user data and does not disclose the storage of erase block management data in the control data sections of a subset of sectors of an erase block as disclosed in Applicant's claims 20 and 42. As such, Matsuo et al. fails to teach or disclose the erase block management structures of independent claims 20 and 42. The AAPA also fails to teach or disclose the erase block management structures of independent claims 20 and 42. The Applicant therefore maintains that claims 20 and 42 are allowable over Matsuo et al. and the AAPA, either alone or in combination. As claims 21, 22, and 49 depend from and further define claims 20 and 42, respectively, they are also deemed to be in condition for allowance.

Applicant respectfully contends that claims 21, 22 and 49 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 21, 22 and 49.

Claims 1 and 3 were rejected under 35 U. S. C. § 103(a) as being unpatentable over AAPA, in view of Sassa et al. Applicant respectfully traverses this rejection and feels that claims 1 and 3 are allowable for the following reasons.

Applicant respectfully disagrees with the Examiner and notes that, as stated above, Sassa et al. fails to teach an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. As such, Sassa et al. fails to teach or disclose the erase block management structure wherein an erase block management structure is formed into the control data sections of the first six sectors of each erase block as disclosed in independent claim 1. The AAPA also fails to teach or disclose the erase block management structures of independent claim 1. The Applicant therefore maintains that claim is allowable over Sassa et al. and the AAPA, either alone or in combination. As claim 3 depends from and further defines independent claim 1, it is also deemed to be in condition for allowance.

Applicant respectfully contends that claims 1 and 3 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1 and 3.

Claim 2 was rejected under 35 U. S. C. § 103(a) as being unpatentable over AAPA in view of Sassa et al., and further in view of Duke. Applicant respectfully traverses this rejection and feels that claim 2 is allowable for the following reasons.

Applicant respectfully disagrees with the Examiner and notes that, as stated above, Sassa et al. fails to teach an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. The AAPA also fails to teach or disclose the erase block management structures of independent claim 1. The Applicant therefore maintains that claim is allowable over Sassa et al. and the AAPA, either alone or in combination. As claim 2 depends from and further defines independent claim 1, it is also deemed to be in condition for allowance.

Furthermore, in order to support a rejection under 35 U.S.C. § 103(a), Sassa et al.'s principle of operation would have to be modified. The Applicant maintains that Sassa et al. teaches storage of identical copies of management information in each redundant area of each memory block of an erase block in the interest of speed, reduction of initialization time, and redundancy. Applying the 1's complement data storage of Duke to the management information storage of Sassa et al. would change Sassa et al.'s principal of operation. Therefore, Sassa et al. cannot be used to support a rejection under 35 U.S.C. § 103 because MPEP § 2143.01 provides that if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious.

Applicant respectfully contends that claim 2 as pending has been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claim 2.

Claims 50-51 and 30-31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sassa et al., in view of AAPA. Applicant respectfully traverses this rejection and feels that claims 50-51 and 30-31 are allowable for the following reasons.

Applicant respectfully disagrees with the Examiner and notes that, as stated above, Sassa et al. fails to teach an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. As such, Sassa et al. fails to teach or disclose a method wherein an erase block management structure is formed into the control data sections of a subset of sectors of each erase block as disclosed in independent claim 50. The AAPA also fails to teach or disclose the erase block management structures of independent claim 50. The Applicant therefore maintains that claim 50 is allowable over Sassa et al. and the AAPA, either alone or in combination. As claim 51 depends from and further defines independent claim 50, it is also deemed to be in condition for allowance.

As also stated above, as Sassa et al. fails to teach an erase block management data structure that resides in the control data sections of a subset of sectors of each erase

block, it fails to teach the Flash memory device of the system of independent claim 26. The AAPA also fails to teach or disclose the erase block management structures of independent claim 26. The Applicant therefore maintains that claim 26 is allowable over Sassa et al. and the AAPA, either alone or in combination. As claims 30 and 31 depend from and further define claim 26, the Applicant maintains that claims 30 and 31 are also deemed to be in condition for allowance.

Applicant respectfully contends that claims 50-51 and 30-31 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 50-51 and 30-31.

## CONCLUSION

In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims.

The Examiner is invited to contact Applicants' representatives at direct dial (612) 312-2211 if there are any questions regarding this Response or if prosecution of the present application may be assisted thereby. No new matter has been added and no additional fee is required by this response.

Respectfully submitted,

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